Fin-Width Effects on Characteristics of InGaAs-Based Independent Double-Gate FinFETs

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***Abstract*— We report the characteristics of InGaAs-based independent double-gate FinFETs with Al_2O_3/$LaAlO_3$ as gate dielectric. The device can be operated in three different modes (*i.e.,* single-, double-, and independent double-gate) made possible by the physically separated two sidewall gates. When the device is operated in the double-gate mode, it exhibits better performance in terms of the On/Off current ratio, subthreshold swing, Off current, and channel mobility than in the single-gate mode. In addition, independent double-gate operation makes it possible to modulate channel properties by applying a bias at the opposite gate via gate coupling effects. Our systematic measurements reveal that gate control and coupling effects are enhanced with reduced fin width.**

***Index Terms*— InGaAs, FinFET, MOSFET, double-gate, carrier distribution, coupling effects, threshold voltage modulation.**

I. Introduction

HIGH drive current, low power consumption and co-integration of various functionalities become the main stream in today's VLSI circuit and system design due to the increasing demand for portable electronic devices and embedded systems. In this perspective, good gate control and dynamic threshold voltage V_{TH} modulation (*i.e.*, high V_{TH} in Off-state and low V_{TH} in On-state) have recently been explored to reduce power consumption and integrate different functions on the same chip [1], [2]. On the other hand, high-electron-mobility InGaAs MOSFETs with advanced structure and *high-k* gate dielectrics have been extensively investigated [3]–[8] to boost carrier transport and drive current. However, the off-state current tends to be too high for the next generation transistors because of the narrow bandgap [9], [10], causing high power consumption. Although many researches have been attempted to ameliorate gate control and reduce off-state current [3]–[8], they have not fulfilled the requirements for circuit applications.

In this letter, we report the results of InGaAs-based independent double-gate (DG) FinFETs. Unlike SOI planar DG structures [11], [12], we employed a 3-dimensional device structure to achieve perfectly aligned two sidewall gates. Our work shows that the device offers better subthreshold swing, lower off current, improved On/Off ratio, and enhanced channel carrier mobility by the use of DG FinFET architecture. In addition, the two separated sidewall gates enable the possibility of modulating the channel properties such as threshold voltage and carrier mobility through gate coupling effects. Our measurements have revealed that the device characteristics and coupling effects strongly depend on the fin width W_F. We have observed enlarged coupling effects compared to the Si-based DG device [11], which means that the InGaAs DG device is a good candidate for dynamic threshold voltage control.

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II. Device Fabrication and Experiments

A scanning electron microscope (SEM) and a schematic cross-section image of the InGaAs DG FinFET studied in this work are shown in Fig. 1. A p-doped (1×10^{18} cm^{-3}) InP substrate was used as the starting material to reduce subthreshold leakage and prevent punch-through. The thickness of the InGaAs film grown on (100) InP was 150 nm, which defined the fin height H_F. The content of In and p-type doping concentration of the InGaAs are 0.53 and 2×10^{16} cm^{-3}, respectively. The source and drain regions were formed by the Si ion-implantation followed by 600 °C anneal to activate the implanted dopants. Next, the fin etching was performed by BCl_3/Ar high density plasma etching (HDPE) followed by surface cleaning in buffered oxide etch (BOE) and diluted $HCl:H_2O_2$ solution. The InGaAs channel release process was conducted using $HCl:H_2O$ (1:2) solution. The InGaAs fins were defined along <100> direction. More detailed InGaAs fin pattern process used in this study is reported elsewhere [13], [14]. The typical angle of the trapezoid shaped InGaAs fin-structure is around 75° after HDPE etching. The two separated sidewall gates were formed by a single lithography step. An Al_2O_3 (1 nm) and $LaAlO_3$ (9 nm) layers

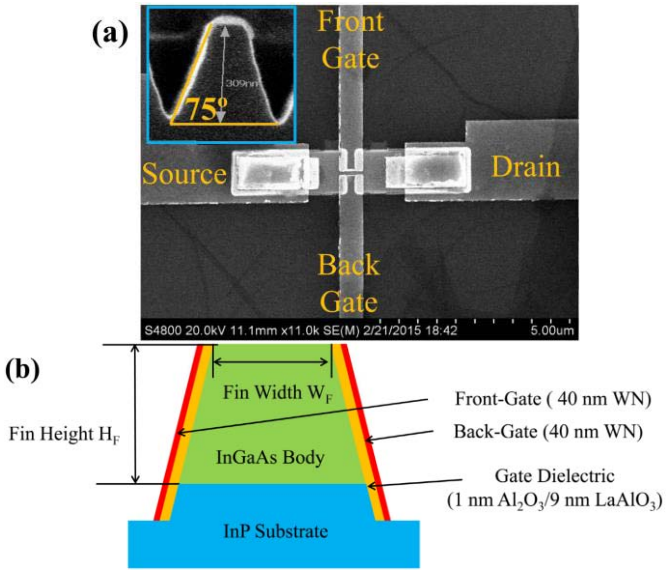

Fig. 1. InGaAs double-gate FinFET structure. (a) SEM and (b) schematic cross-section image of the processed device. Inset in Fig. 1(a) shows the cross-section SEM image after fin definition.

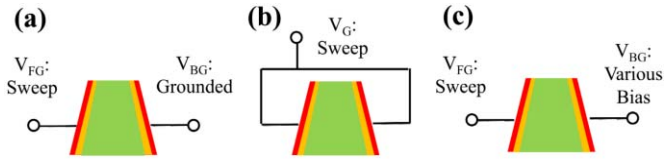

Fig. 2. Schematic description of bias conditions for three different operation modes. (a) Single-, (b) double-, and (c) independent double-gate mode.

were stacked by atomic layer deposition (ALD) on InGaAs as the gate dielectric. The equivalent oxide thickness was determined to be 2.64 nm. A 40 nm-thick WN was deposited as the metal gate. Electron beam lithography was performed to open the fin-top window followed by WN dry etch on the top of the fin, achieving two sidewall gates. Au/Ge/Au/Ni/Au and Ni/Au were used for the source and drain Ohmic contact and gate electrode, respectively. DG FinFETs with various W_F (down to 20 nm) and gate lengths L_G (down to 180 nm) were fabricated to investigate the geometrical effects. Each transistor was composed of a single fin as shown in Fig. 1(a).

For device characterization, we investigated three different operation modes. In the single-gate (SG) mode (Fig. 2(a)), the back-gate was grounded while the front-gate was swept. On the other hand, the same bias was applied to the front- and back-gate by connecting the two gates together, in DG operation (Fig. 2(b)). In Fig. 2(c), the front-gate was swept with various back-gate biases in the independent DG mode.

Sentaturus 3-D simulation [15] was conducted to give a detailed account the front-channel carrier mobility dependence on the back-gate biasing. Poisson and electron continuity equations, and simplified quantum model provided by the simulator were applied to study the conduction mechanisms based on the electron drift-diffusion theory.

III. Results and Discussion

In the SG mode, the $I_D(V_{FG})$ curves were measured in the linear regime (V_D = 20 mV). Fig. 3 shows the effect of

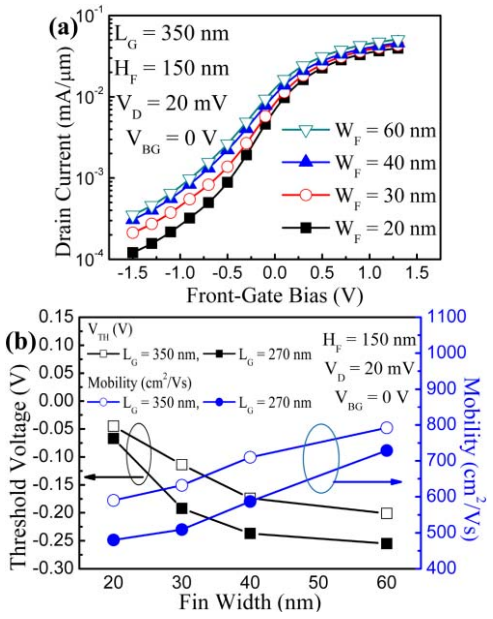

Fig. 3. Typical device properties in single-gate mode. (a) Drain current versus front-gate bias for various fin widths. (b) Front-channel threshold voltage and carrier mobility versus fin width.

the W_F on the basic device characteristics. In Fig. 3(a), the thinner W_F device shows better subthreshold swing and lower off current due to the enhanced gate control. To quantify the device performance, the front-channel threshold voltage V_{THF} and carrier mobility μ were extracted from the *Y-function* [16]: $Y = I_D/\sqrt{g_m}$. Fig. 3(b) shows that V_{THF} increases with decreasing W_F. When the W_F decreases, the conduction band energy increases due to the quantum confinement effects [17], requiring a higher gate bias to achieve inversion, thus increasing V_{THF}. In addition to this phenomenon, the prevention of the back-interface leakage current aggravates the threshold voltage increase. In a thinner device, the surface roughness scattering is enhanced, and the carrier mobility deteriorates. Note that in shorter device the V_{THF} is lower since the leakage current at the back-interface is enhanced. This threshold voltage reduction is less for the thinner fin width due to the suppression of the leakage current.

We have compared the device characteristics in both SG and DG modes. In the DG operation, the on-current is higher by activating the two side-channels, while the off-current is lower (Fig. 4(a)). As shown in Fig. 3(b), V_{THF} is negative, because there is a current path at the back-interface in the SG mode. However, in the DG mode, the off-current is suppressed by the back-gate bias. As a results, the On/Off ratio is ameliorated. In the DG mode, the potential distribution inside the body is more uniform, and gate control is enhanced by using the two gates simultaneously, giving rise to better subthreshold swing. The control of the gate is further strengthened by reducing W_F, just as in the SG mode. Fig. 4(b) and (c) compare the V_{TH} and μ for the two different modes. In the DG mode, the device exhibits higher V_{TH} due to the better gate control that blocks the back-channel current. The carrier mobility is also increased in the DG mode, because the centroid of the inversion carriers is moved toward

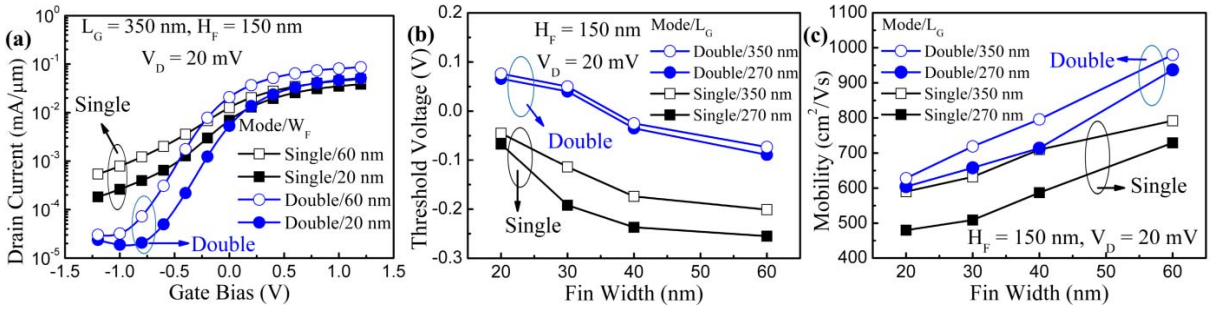

Fig. 4. Comparison between single- and double-gate modes. (a) Drain current versus gate bias. (b) Threshold voltage, and (c) carrier mobility versus fin width.

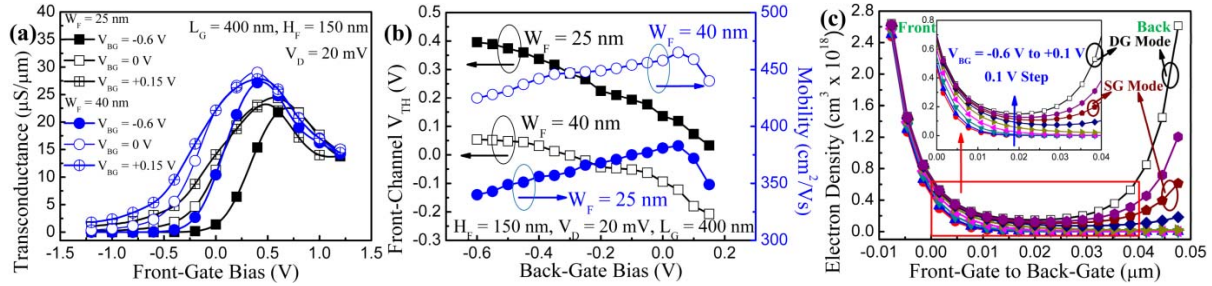

Fig. 5. Coupling effect in an independent double-gate transistor. (a) Transconductance versus front-gate bias for various back-gate biases. (b) Threshold voltage and carrier mobility versus back-gate bias extracted by *Y-function* and $g_{m,max}$ method: $\mu = (L_G g_{m,max})/(W_G C_{ox} V_D)$ [21], respectively. (c) Electron distribution at $V_{FG} = +0.4$ V and $W_F = 35$ nm for various back-gate biases. Electron distribution was taken at 50 nm away from the top of the fin. Open symbol (black square) shows the electron distribution at $V_G = +0.4$ V in DG mode. Electron distribution in SG operation is the same as in independent DG mode at $V_{BG} = 0$V.

the middle of the InGaAs body due to the lessened lateral electric field between the two gates [18]. Therefore, the surface roughness scattering is reduced and the mobility is enhanced.

For the gate coupling effect investigation in Fig. 5, we measured the drain currents at various back-gate biases. When the back-channel is changed from accumulation to inversion, the body potential is increased [19], and V_{THF} is reduced (Figs. 5(a) and (b)). Note that the on- and off-currents are comparable to those of the DG mode when the back-channel lies in accumulation and inversion, respectively ($I_{off} = 1.89 \times 10^{-5}$ mA/μm @ $V_G = -1$ V in DG mode, and $I_{off} = 1.48 \times 10^{-5}$ mA/μm @ $V_{FG} = -1$ V and $V_{BG} = -0.3$ V in independent DG mode). This coupling effect depends on W_F, as shown in Figs. 5(a) and (b). In a thinner device, the V_{THF} is more sensitive to the back-gate bias due to the higher body capacitance [19]. In an InGaAs DG transistor, the coupling effect is larger than the SOI DG structure [11]. In SOI-based technology, a 67 mV/V of coupling coefficient defined as $\Delta V_{THF}/\Delta V_{BG}$ was reported in 5 nm of rectangular body thickness and 100 nm of gate length device [11]. A 155 mV/V (@ $W_F = 25$ nm and $L_G = 400$ nm) of coupling coefficient was achieved in InGaAs DG FinFETs even if body thickness (*i.e.*, W_F) was 5 times thicker (@ $W_F = 25$ nm) and gate length was longer (@ $L_G = 400$ nm) than that of SOI DG. We believe that the coupling effects should be enhanced in InGaAs DG FinFETs with further decreasing of W_F and L_G due to the higher body capacitance and deteriorated gate control, respectively. From the circuit application perspective, the strong modulation of the front-channel by the back-gate bias is important, because it enables dynamic threshold voltage control.

In Fig. 5(b), the front-channel carrier mobility depends on the back-gate bias [20]. When the back-gate bias is negative, the electric field between the gates is strong. Therefore, the centroid of the inversion carriers are located near the front-interface, as shown in the simulation results (Fig. 5(c)), causing strong surface roughness scattering, and lower carrier mobility. With increased back-gate bias, the surface roughness scattering decreases, and carrier mobility rises since the inversion carrier density at the middle of the InGaAs body is increased. When the back-channel is in strong inversion, the back-channel carrier density is increased and scattering is enhanced near the back-interface, deteriorating carrier mobility.

IV. Conclusion

We have demonstrated the DG FinFET concept and coupling effects by the use of an InGaAs transistor body. Compared with the SG mode, the DG operation offers better device performance and gate control in terms of subthreshold swing, On/Off current ratio and carrier mobility. The gate control is improved by reducing the W_F. We have achieved stronger gate coupling effects in InGaAs DG devices than in SOI-based DG structures. The front-channel parameters such as V_{TH} and μ can be beneficially modulated by the back-gate bias. Moreover, the coupling effect is enhanced with decreased W_F. Therefore, the InGaAs independent DG FinFET is a suitable device for dynamic threshold voltage control.

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